ADVANCING SEMICONDUCTOR LEADERSHIP IN AMERICA

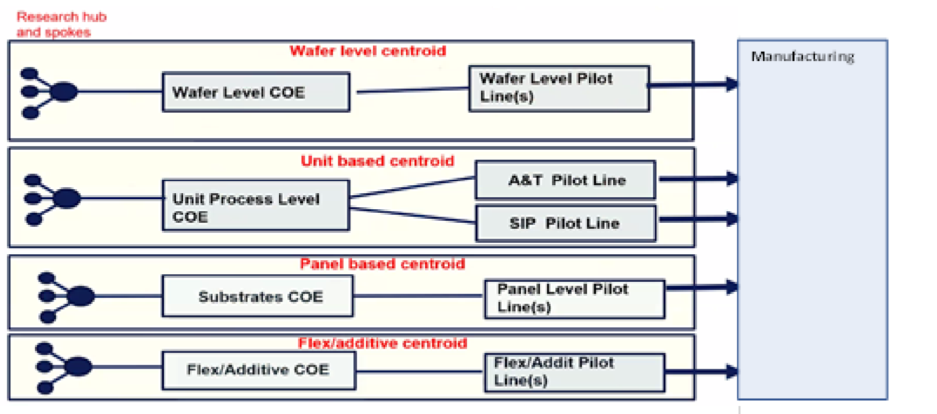
Recommendations for revitalizing semiconductor research and manufacturing through the National Advanced Packaging Manufacturing Program

March 2023

Executive Summary

The formation of the NAPMP is critical for the recovery of advanced semiconductor packaging technology and manufacturing in the US, with the ultimate goal that in the next decade the US will lead the world in the design, technology and production of advanced semiconductor packaging. Following guidelines from NIST/DOC, the NAPMP will be structured as a combination of project-centric Coalitions of Excellence (COEs) and Pilot Lines that will transition new technologies to domestic and sustainable manufacturing. The NAPMP's three major initiatives are: (i) work closely with and support packaging research, (ii) accelerate packaging technology development, and (iii) transition these technologies into economic and sustainable manufacture in the US such that the cost structure for packaging manufacturing undergoes a revolutionary change. The advent of heterogeneous integration, combining different chips or chiplets into one package, provides the ideal inflection point to establish a strong domestic capability.

The NAPMP will be structured around five pilot lines, each working on a different packaging form factor (wafer based, panel based, system in package (SiP), unit based and flex). Each pilot line will be supported by COEs that focus on identifying and managing technology programs that feed into the pilot lines for experimental verification and manufacturing hardening as shown schematically below:



The NSTC and NAPMP should be structured to share administrative functions (BOD, CEO, legal, contract, personnel etc.) but have separate and clearly defined program budgets, funding and control and individual Technical Advisory Boards under their own respective COOs.

This white paper proposes that COEs operate through carefully chosen and managed projects on different packaging technologies (wafer level, panel level, unit level and flexible circuits) to enable multiple expanding industries (lower energy data centers, memory centric computing, defense/aerospace, 6G mobile, autonomous driving, AR headsets, renewable energy, EVs, medical devices) which will require advanced packaging. Two of the COEs and one of the pilot lines will be located at Manufacturing Institutes. The ultimate focus of the COEs/pilot lines will be economic and environmentally sustainable US domestic manufacturing.

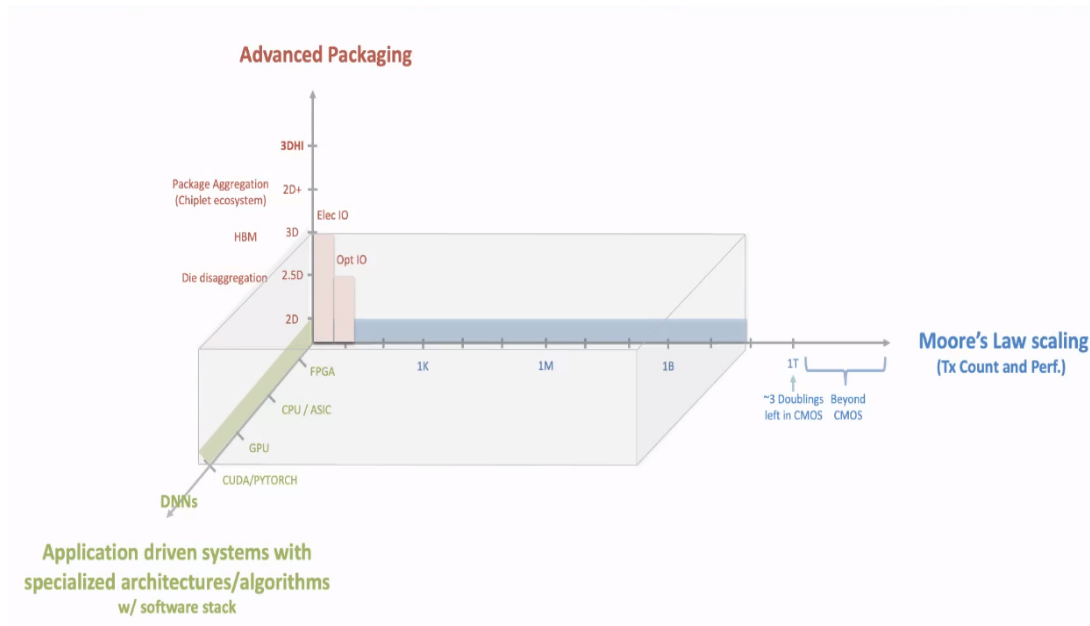
The NAPMP facilities will collaborate closely with university and commercial research, with the NSTC and other government-supported activities such as NIST and ME Commons. The NAPMP will work with the NSTC to build a national workforce development program using its facilities to offer intern and apprenticeship opportunities to build the skilled workforce required for manufacturing in the US.

Introduction

The challenges faced by the US semiconductor industry over the past twenty years have been well documented:

- Loss of US produced market share (down to 12% for fabs and 3% in packaging)
- The slip in advanced digital electronics technology
- The fragility of the semiconductor supply chain and dependence on Asia

In response to these challenges, the US Congress has passed the CHIPS and Science Act, which has allocated $52B to help resolve the challenges described above and to ensure the country's economic and national security. The challenge is particularly acute for semiconductor packaging for two reasons. First, packaging needs are very diverse and there are no large packaging companies or facilities in the US, with the exception of Intel which is mostly vertically integrated. For example, 3nm processors are used both for data centers and cell phones but are packaged in very different modules. Second, as the benefit of reducing transistor size (Moore's Law) is maxing out, advanced packaging will become key to maintaining the extraordinary benefits associated with ever-increasing computer power. This is illustrated in the graphic below which shows the benefit in three dimensions – smaller transistors, advanced packaging and improvements in architecture/algorithms.



While Moore's Law faces increasing challenges and obstacles, advanced packaging will help not only in its own right, but also it will make possible the hardware and design required for the third axis, namely architectures and algorithms.

This white paper is designed to support the efforts of NIST as it prepares to manage and assign the funding allocated for the NAPMP to remedy this situation. The success of the NAPMP will be critical for two reasons:

a. Packaging is about to undergo a major new technology upgrade to enable new applications. This is a critical opportunity for companies in the US to get back into onshore production. The implications of these new packaging technologies will extend far into electronics system assembly.
b. Generally available high-volume packaging production is non-existent in the US. A major effort will be required if this deficiency is to be corrected to create jobs, add resilience to the supply chains and protect our economic and national security.

Grand Challenge and Overarching Goal

The desired outcome of the CHIPS Act is to increase the manufacture of semiconductors in the US, thereby increasing the number of jobs, and improving supply chain resilience and national security. It is recommended that the grand challenge to be solved by the CHIPS Act be defined as follows:

"In the next ten years the United States will lead the world in the design, technology and production of semiconductors"

This white paper focusses on the NAPMP portion of the CHIPS Act funding (section 9906d) and recommends that the NAPMP programs be focused into three broad initiatives:

1. Encourage and support advanced research to create new technologies, designs, tools and products.

Innovation built upon commercial, start-up and university research is a great strength for the US. The NAPMP needs to not only exploit this innovation by using CHIPS Act funding to provide the facilities to enhance the transition of successful ideas into production in the US, but also to proactively fund and encourage fundamental research in areas related to semiconductor packaging to assure that the United States maintains leadership in the future. This requires the NAPMP, along with its partners, to engage in comprehensive road mapping and planning for packaging technologies looking out ten year or more. This would also enhance the NAPMP's role in aligning various organizations and companies involved in advanced packaging.

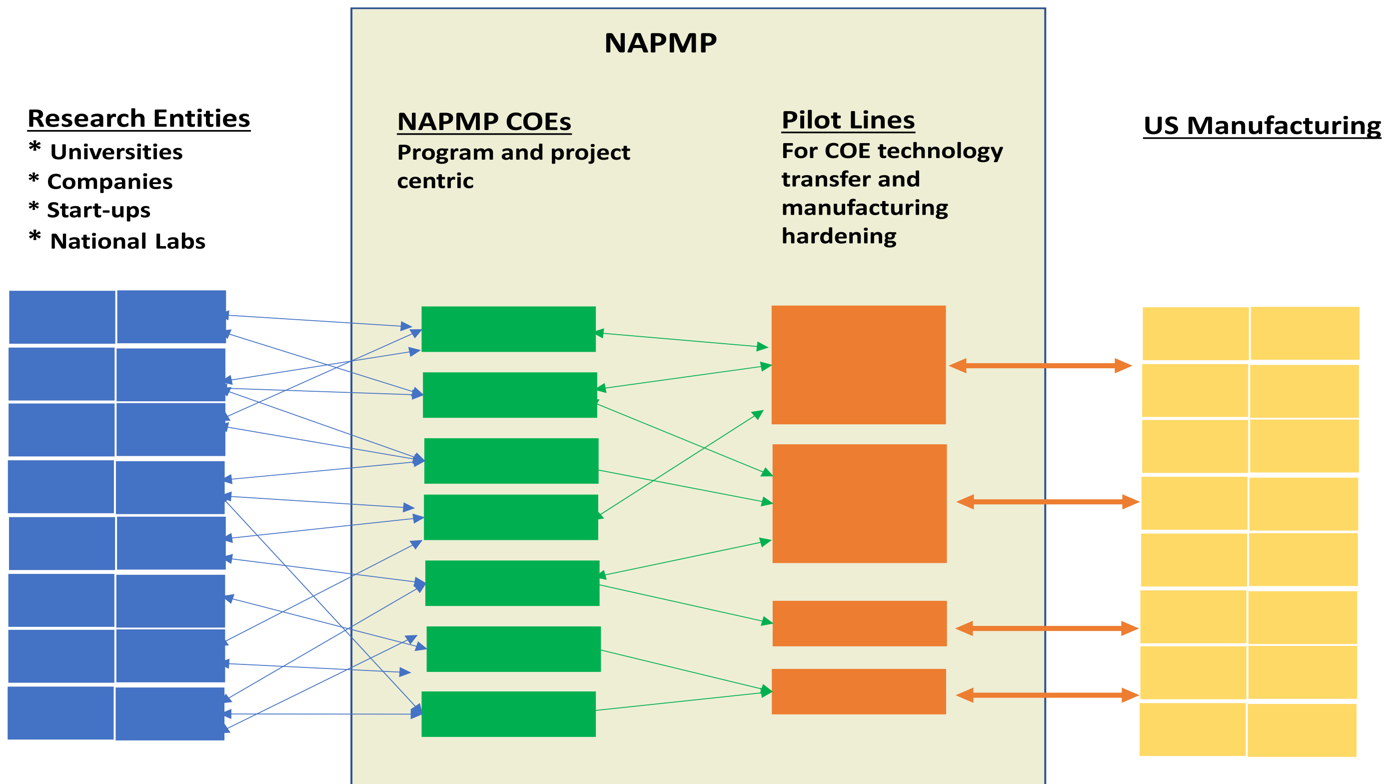
2. Accelerate technology development.

Development projects, unlike research, are usually well understood in terms of both physics and market need. The NAPMP needs to accelerate existing industry roadmaps compressing time frames. For example, a ten-year roadmap would be condensed to five years, while ensuring the technologies result in economic manufacture in the United States. This is the only way the US can catch up and lead the world in packaging materials, assembly tools and technology again. It is also critical that all development projects have a clear path for success defined in advance.

3. Transfer to Commercial Production

This is less well defined but is an important challenge. The commercial landscape is very diverse. However, regardless of what is implemented in items 1 and 2 above, there needs to be significant input and direction from commercial entities – materials, equipment, device manufacturers and their fabless customers – and a viable plan for introducing the new technologies into production in the US. Without this transfer to manufacturing there is a risk that the R&D will simply be exported to production lines outside the US.

The NAPMP would be structured with interacting COEs and pilot lines, each focused on a particular technology or packaging form factor as shown in the figure on the following page:



It is crucial that NSTC and NAPMP COEs and pilot lines provide a smooth glide path for innovations into US manufacture. The capital cost and access to a full suite of semiconductor packaging and assembly tooling is very expensive and beyond the scope of most companies in the industry ecosystem. At the same time, semiconductor manufacturing companies are justifiably loath to allow untried materials into their fabs and can also be proprietary over experimental results. The NSTC and NAPMP organizations must fill this gap.

Key large market segments that can benefit from advanced packaging

There are several large market segments which will benefit greatly from access to advanced packaging. These markets will be the driving force for package manufacturing re-shoring to the United States. These market segments closely align to the ASIC-proposed NSTC COEs and would have their specific packaging needs supported by the NAPMP. To assure close interaction between the NAPMP and the NSTC Vertical COEs, it is recommended that two application engineers from the NAPMP be assigned and located at each NSTC Vertical COE.

It should be noted that not all these markets are high volume/low mix but rather are high mix/low volume; nevertheless, there are important opportunities to both support existing low volume packaging facilities in the US and to re-shore some packaging with appropriate flexibility in manufacturing.

1. High performance computing for low energy data centers (NSTC Advanced Logic COE)

Data centers largely built around high-performance computing and memory devices have shown explosive growth in the past few years, up 30% in 2021 and 50% in 2020. This growth is expected to continue for the next decade. However, this growth comes with an equivalent increase in energy consumption, and it is imperative that the energy efficiency be improved by packing the chips more closely together and using photonic interconnects. Technology advances in semiconductor packaging (3D heterogeneous integration (3DHI), hybrid bonding and co-packaged

photonics) will help with both performance and to reach an ambitious target of a thousand times reduction in energy use.

2. Data communication, autonomous driving LIDAR and AR reality headsets (NSTC Analog/Mixed Signal COE)

To gain full advantage of the performance of advanced logic devices, they need to be connected to high-capacity communication links to move data at the required speed. Laser based optical communication is moving from long haul fiber optic networks all the way back to the circuit boards and the advanced logic packages. The integration of these photonic links with semiconductor devices is an area of rapid development and an opportunity for onshore production.

The use of LIDAR for autonomous driving is also an opportunity for integrated photonics as the lasers and detectors need to be coupled to high performance computing and massively parallel data streams. Autonomous driving applications could be very large, with automobile companies pulling these high value-added systems into their US based manufacturing.

The rapidly growing market for AR headsets incorporates a variety of planar optics and waveguides, which are manufactured largely using silicon-based thin film technology. Recent innovations have leveraged silicon photonics on glass. Packaging the electronics and optical components into small and light headsets will offer a significant market for co-packaged electronics and optics.

3. Memory centric computing (NSTC Memory COE)

Von Neumann computer architectures are beginning to suffer performance restrictions given the need for very rapid transfer of data between memory and processors. There is an increasing demand for co-integrated and co-optimized compute memory structures, including neuromorphic designs. These new memory/compute systems will draw on the 3D HI described above. Given that 85% of all transistors manufactured are used in memory, and the market growth rate exceeds 15% CAGR, it is critical that this market segment is well supported. The advent of new memory centric computing architectures and systems will have a dramatically beneficial impact on data processing, artificial intelligence and edge computing throughout the United States.

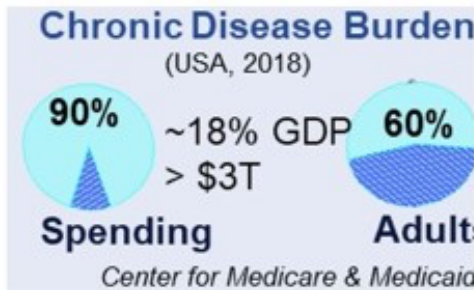
4. High frequency electronics for defense/aero, autonomous driving, 6G base stations (NSTC Analog/Mixed Signal COE)

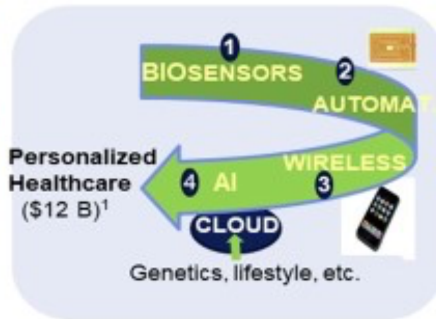
The availability of mmWave/Sub-THz (>60GHz) advanced RF System-in-Package technology will drive a variety of industries including defense and aerospace for advanced radar and targeting systems, 6G mobile communication base stations and electromagnetic imaging for autonomous driving systems. The RF technology and packaging needs differ from other semiconductor packaging in that they are much more heterogeneous (use of different materials for high frequency, compound semiconductors which come on wafers less than 300mm, embedded antennas etc.) in addition to using the very dense packaging obtained using 3D HI for silicon devices. This important market and technology segment will need its own focus.

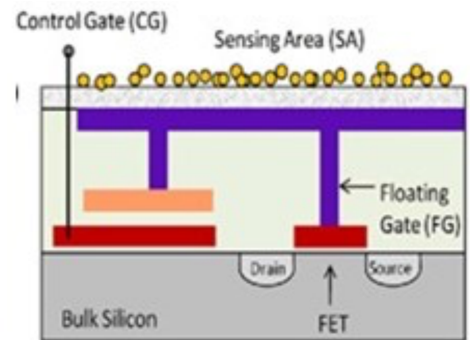
5. Medical devices (NSTC Bio/Med COE)

Electronic, photonic and magnetic devices are finding increasing importance for medical care. With the increasing occurrence of chronic diseases such as diabetes, hypertension and cardiac disorders, and the move towards earlier diagnostic and treatment to reduce healthcare costs, there is a tremendous opportunity for high-volume, low-cost medical devices over the next decade, including the use of MEMS structures for "lab on a chip," implants and drug delivery with opportunities for sensors that can detect problems through the analysis of sweat or saliva. Developing

low-cost packaging materials which are miniaturized, bio-compatible, capable of near-field wireless communication and use very low energy along with the required battery technology will be a challenge.







6. Electric Vehicles (EV) and Renewable Energy

EVs and renewable energy are rapidly growing markets, essential to support the reduction in the use of fossil fuels. Both will require much higher voltages and power levels than typical semiconductor. Developing safe and reliable packaging able to handle the voltages and powers, even in extreme environments, will be an important enabler of these markets. It should also be noted that EVs typically have twice the semiconductor content (~$800 vs $400) as internal combustion automobiles.

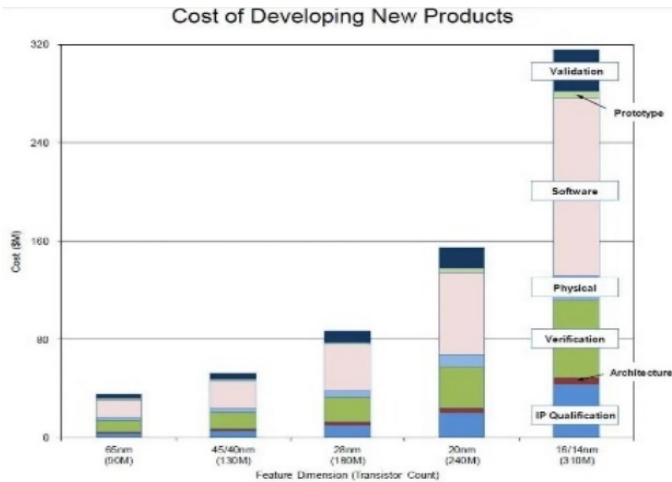
To support these key market segments, the NAPMP should consider creating several COEs to cover the full range of packaging technologies required to support new opportunities, including interfacing with research organizations and transferring this technology to commercial manufacturing. These COEs, which will each be theme focused (e.g. 3D HI, RF, etc.), will define, fund and manage a set of roadmaps and projects inside their overall scope of technology. It is expected that the COEs will be project/program centered, jointly funded by industry partners, and would not have significant new facilities, but would use existing locations and organizations that closely link with their technology focus.

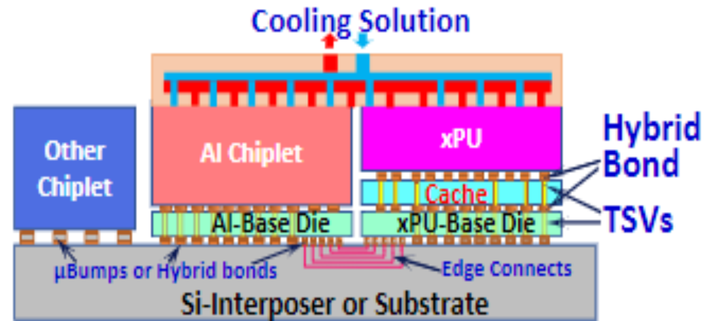
Impending Packaging Technology Changes

There are several new packaging technologies that will enable the market opportunities described in the prior segment and offer an opportunity to restart high volume semiconductor packaging in the US. The NAPMP would be organized around a set of COEs which would each address a major packaging technology change. NSTC/NAPMP COEs would work together to build a variety of "demonstrators" in each major segment to prove in the new technologies and assembly tooling to shake out any issues with realistic modules. The proposed COEs are as follows:

3D Heterogeneous Integration COE (this is described in more detail as an example of the COE objectives and execution)

The productivity in semiconductor devices that has driven electronics so much for the past fifty years is beginning to run out of steam. Device dimensional scaling and lithography improvements are beginning to slow, plus the complexity of the state-of-the-art devices is causing their design to become cost prohibitive in terms of cost and time, as shown on the following page:





Instead of large monolithic custom ICs, the industry is moving to the use of smaller “chiplets” that need to be interconnected to each other in dense 3D HI packages, as shown above, to essentially mimic the interconnect dimensions as if they were a single chip. This would provide a large reduction in energy consumption and enhance computing speed. This will require upfront and rigorous co-design between all aspects of silicon design, fabrication, packaging and test. The packaging technology would be developed in the NAPMP 3D HI COE using a set of specific projects such as (i) extending wafer finishing process and equipment for down to 2um bond pitch, (ii) hybrid bonding with cost of ownership (including yield) compatible with US manufacture, (iii) thermal control systems, (iv) metrology/inspection of 3D assemblies, (v) reliability issues for 2um bond pitches, and (vi) building a functional 3D module to demonstrate full integration. Each project would be required to have industry participation and funding to assure that the required industrial interest does in fact exist.

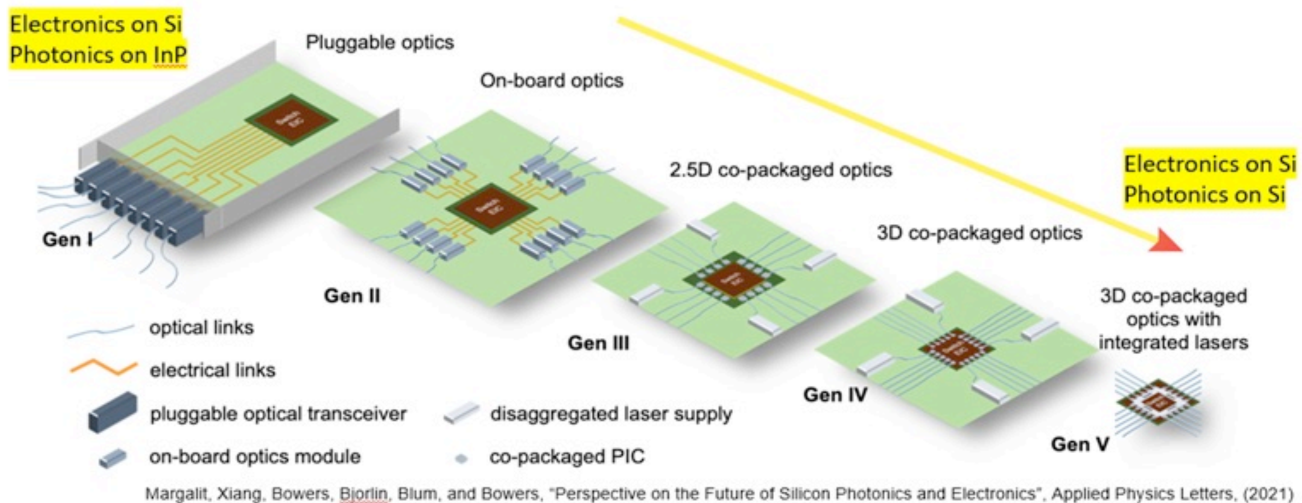
This technology, while in its infancy with tools capable of 10um bond pitch, is more like back end of the fab technology as opposed to standard device packaging and so offers an opportunity for reshoring manufacturing. It should be mentioned that the famous “Dennard Scaling” that defined that smaller transistors offered less power consumption, higher frequencies and higher density, is moving to an equivalent scaling in packaging offering the same benefits – less power, higher performance and greater density. 3D HI packaging would be applicable to a wide variety of markets including memory centric computing, AI & Edge compute, Defense/Automotive, co-packaged optics, and intelligent sensors.

Achieving success on this roadmap also requires the introduction of advanced materials influencing every step of the hybrid bonding process to enable zero defects and low temperature bonding processes to successfully integrate these late-stage components in a heterogeneous package. Equally critical is the development of thermal management systems that will allow the required heat dissipation from close packed chips. The 3D HI COE would accelerate development of tools, materials and processes, collaborate with the NSTC EDA activities and other COE verticals and assure 3D HI packaging economically can be manufactured in the US.

3D HI packaging technology can enhance the use of chiplets, which themselves can be built from different and optimized design rules/technologies, without losing the performance gained from monolithic integration, allowing the chiplets to be integrated together effectively as “virtually monolithic”. This will allow lower cost development by using new or existing chiplets to build a complete “system in package,” significantly expanding the number of companies that can afford to develop these products. This is often referred to as “the democratization of design” and will play to the strength of the US in innovation and start-up companies.

Co-packaged Photonics COE

The data explosion in internet traffic driven by AI, IOT, cloud computing, content streaming and social networks is driving growth in datacenters. The datacenter product sector is forecast to have revenues continuing to grow at a CAGR of 26%. The coupling of fiber optics with CMOS electronics in close proximity will reduce power requirements and increase bandwidth for the datacenter. A large challenge is reducing interconnect lengths and bringing the optical signal closer to the CMOS logic devices. Photonic components, including photonic integrated circuits (PICs), lasers, modulators and transceivers, are used to build this fiber-optic infrastructure. To reduce power, electrical interconnects need to be reduced and replaced with optical connects where possible. Co-packaged optics is advanced packaging where fiber, transceivers and electronics are brought together in a single package to reduce the electrical interconnects. The scaling of the interconnects and migration to 2.5D and 3D HI co-packaged optics in the data center is required for increasing bandwidth in the data center. The co-packed optics scaling is illustrated below and it is fundamentally important for increasing bandwidth and reducing power in the data center.



Margalit, Xiang, Bowers, Bjorlin, Blum, and Bowers, "Perspective on the Future of Silicon Photonics and Electronics", Applied Physics Letters, (2021)

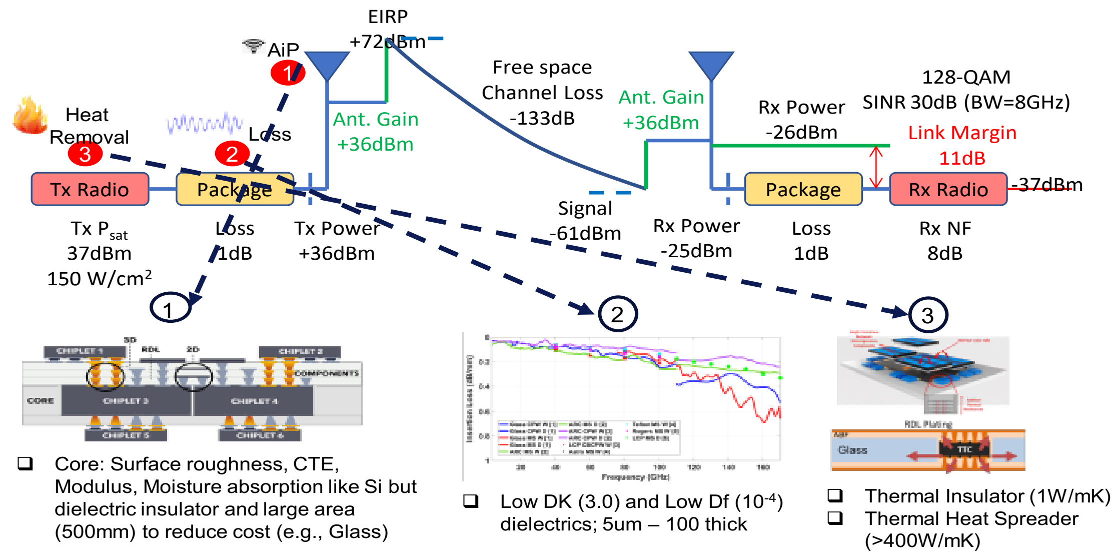
Augmented reality headsets incorporate a variety of planar optics and waveguides manufactured largely using silicon-based thin film technology. Packaging the electronics and optical components into small and lightweight headsets will offer a significant market for co-packaged electronics and optics. Closely related is the need for high density micro-LED for AR/VR and high-resolution display technologies. This technology can integrate multi-color GaN pixels onto silicon backplanes either through high-speed/high precision pick-and-place or via reconstituted wafers (similar to Fan Out Level Wafer Packaging) being hybrid bonded with a silicon backplane.

System in Package (SiP) COEs

SiPs are a very diverse grouping but are a particularly important area in semiconductor packaging. As packaging techniques offer increasing density, power efficiency and performance, a greater fraction of system assembles will be taken over by SIPs having a significant impact on the electronics assembly industry. SiPs often consist of a multiplicity of different components and in this regard are somewhat different from 3D packages described above.

There would be several areas of focus for this group of COEs. One particularly significant area of expansion is the use of SIPs for high frequency technologies. A wide variety of commercial applications are taking advantage of the high frequency electromagnetic spectrum in excess of 60GHz. These include mobile communications (6G), defense and aero (various), augmented reality and radar imaging for the automobile industry. This will need high

performance, highly reliable packaging materials and substrates that are compatible with the required frequency transmission but also the complexities of hybrid integration of multiple components such as integrated antenna in package and embedded dies. The complexity of 6G SiPs is illustrated below:



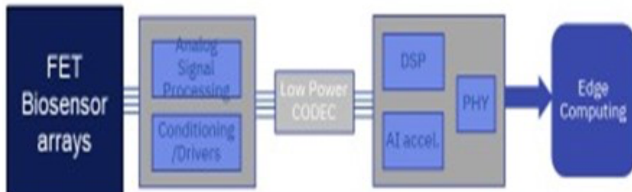
A second area is the need for high voltage/high power. The requirements for EVs and the power grid encompass voltages and power levels far beyond that used for digital electronics – up to 15kV and >1MW. In addition, these power modules frequently use semiconductor materials such as SiC, GaN and Ga_2O_3 as well as Si further complicating the package assembly. In consequence, special techniques are required for packaging these power modules, including the ability to handle wider temperature ranges (-40^{0}C to 150^{0}C) and more effective cooling techniques, such as liquid or two phase rather than air heat sinks.

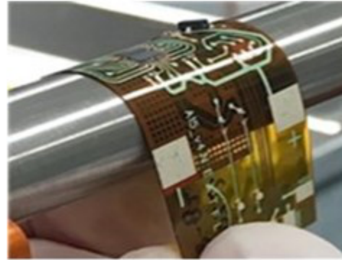
A third COE is for micro-electromechanical systems (MEMS). These devices draw on silicon and glass/silica micromachining process capability to build physical small devices (some use flexible substrates that would be handled by the Flex COE). Rather than operate only on electrical signals these MEMS devices use mechanical, chemical, and optical phenomena and signals to interact with the environment. As a result, they also have specialized packaging requirements that include hermetic packaging with broad accessibility for electrical, fluidic, optical and mechanical. The package provides protection from the environment while enabling device functionality in a variety of environments. The MEMS projects will focus on the multiplicity of specialized packaging needed for MEMS structures to assure that many different applications (medical, auto, communications, GPS, defense, etc.) are available and economically manufactured in the US.

A fourth area is fanout wafer level packaging (FOWLP), which enables multiple devices to be integrated together in a single chip-scale package. This packaging technology is based around embedding die in epoxy mold compound rather than using a conventional substrate, and uses redistribution and bump interconnect technologies similar to wafer level packaging applications to interconnect the devices within the package. Used in RF, power management ICs, baseband processors, and high-end servers, FOWLP can support high frequency applications for 5G/6G and aerospace and defense as well as other analog, digital, and mixed signal SiP applications. FOWLP projects would be focused on establishing wafer-level domestic manufacturing capability and advancing the technology to support higher levels of in-module integration.

Flex and Additive COE

This technology uses the additive nature of printing the interconnects and circuit for a system design and combines it with direct die attach of thinned die to create new, low-cost, lightweight, flexible designs as shown below with applications in medical/wearables, aerospace, military, automotive and more. A sweat analysis module with flexible circuitry showing interconnections and attached thinned die is shown below.





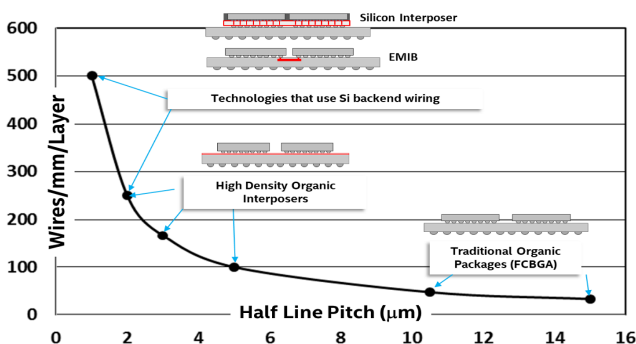
Flex and additive materials and technologies use the sustainability aspects of printing, meaning a much smaller waste stream, fewer processing steps and the ability to print electronic circuits on nearly any surface. The NAPMP COE will use these technologies to extend the interconnection density from the present 1mil down to single digit micron levels, along with laser trimming and an array of assembly capabilities as well as electrical, mechanical, and environmental test tools.

Substrates and Interposers COEs

Semiconductor devices are mounted onto substrates to allow interconnection to the outside world. Substrates are an important pillar of advanced packaging and consist of several different materials (silicon, organic and glass) and come in two distinct form factors – wafer and panel – and as a result use different types of equipment.

We recommend wafer-based interposers be melded in with the 3D COE to make very dense device packages by mounting the chip onto a wafer which has redistribution layers (RDL) to external bond pads. The goal of the projects would be to accelerate the development of the redistribution technology to decrease the L/S dimensions from 10um to 0.8um (increasing the RDL from 55/mm to 480/mm), and increase the number of metal layers from 2 to 6, and increase the number of I/Os from 340/mm^2 to 10,000/mm^2.

Panel based substrates play a crucial role in the overall design of electronic modules by increasing the interconnection density and where each technology has a different role in the interconnection as shown below and would be supported by a combined COE and pilot line.



1. **Interposers**
   Interposers serve as high density integration platforms for interconnecting chips and chiplets in close physical proximity and provide the high bandwidth electrical communication channels between components. Typically fabricated using silicon or glass with inorganic dielectrics and metal routing processes similar to CMOS BEOL or wafer level processes, interposers are usually fabricated on wafers or larger panels. The objectives of the interposer projects would be to increase the capability of interposers by increasing the individual interposer size; utilizing smaller lines, spaces and layer to layer vias (down to <1 micron); routing layers on both sides; developing processes to use glass and other materials; and increasing the size of the panels processed to reduce costs.

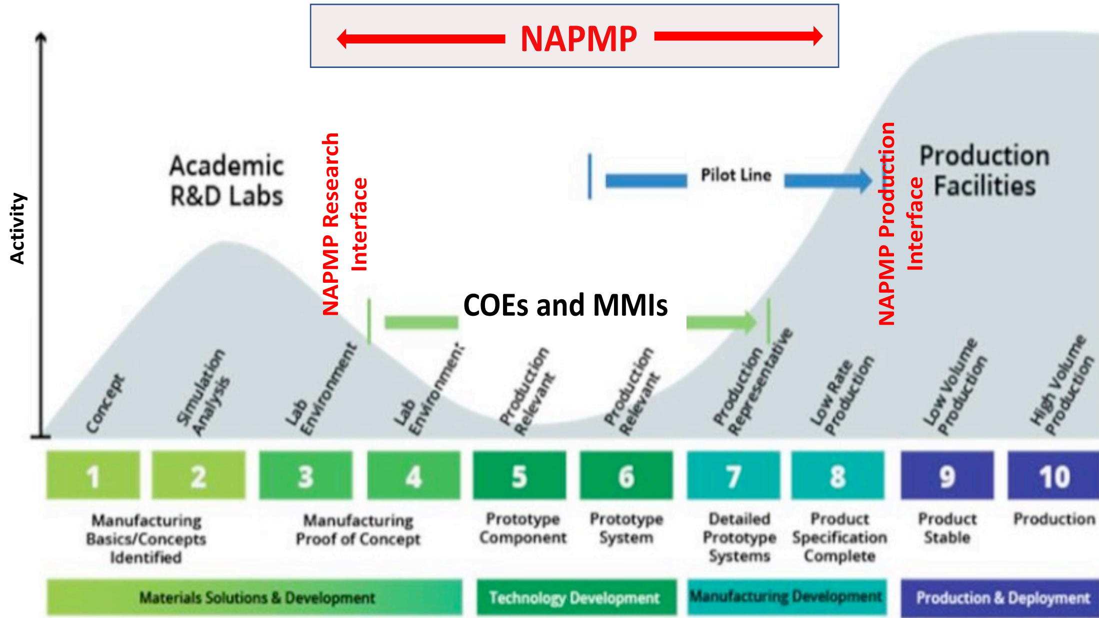
2. **Substrates**
   Substrate interconnections use the largest area substrates. The most widely used are organic materials. Current semi-additive substrate manufacturing processes are significant contributors to the use of dangerous chemicals and generation of hazardous waste at risk of environmental harm. However, as the interconnection dimensions are reduced there is a growing opportunity to use inorganic materials and processes more like the back end of the fab to build high density substrates. The Substrate COE would drive line/space density to <2um by developing new materials and processes to achieve the desired target and reducing environmental impacts. Additionally, advanced substrate technologies can be developed to provide novel die interconnect schemes and high-speed signal I/O approaches.

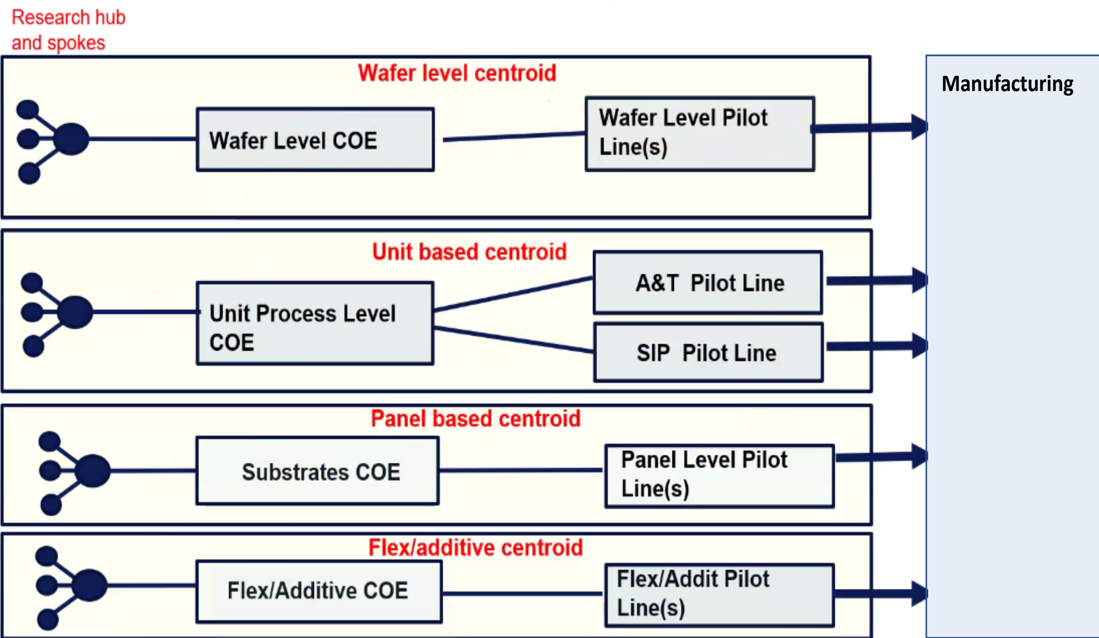
Enabling Domestic Manufacturing

To succeed in establishing domestic manufacturing as dictated in the program name, National Advanced Packaging *Manufacturing* Program, projects and efforts must be focused on developing domestic manufacturing capabilities that have long term economic viability. Current factories are primarily located in lower labor cost geographies due to the high labor content. The rise of heterogeneous integration and advanced packaging in parallel with the establishment of the NAPMP provides a unique opportunity for this transition to domestic manufacturing. Enabling US-based packaging manufacturing (assembly, test, substrates) will require a fundamental redesign of equipment and factories to improve output ten-fold. The lower structural costs will enable more products to be manufactured onshore, since the financial economies of scale require large factories to compete. Re-envisioning tool designs, adopting physical and data standards, creating virtual models of tools and factories coupled with advanced simulation and analytical capabilities are a few examples of the critical work necessary to achieve the critical goal. The broader applicability across a wider breadth of industries is another benefit of this investment and creates significant jobs requiring advanced skills and knowledge. Manufacturing engineering investments in parallel with developing new process flows and packaging architecture is required, otherwise development will be domestic, but manufacturing will continue to be overseas.

How to Organize the NAPMP Advanced Package Development

The proposed role of the NAPMP in transitioning research, accelerating development and transferring technology to manufacturing and its recommended structured is shown below:





The NAPMP technical work would be divided between the five groups of COEs described in the previous section, of which two would be Manufacturing Institutes (AIM Photonics, NextFlex). These COEs would be responsible for accelerating the development of the required technologies, materials and assembly tooling in a time frame less than that of the present industry roadmaps to allow the US to regain the technical lead in packaging. Each COE would also have the responsibility to interface, and fund as appropriate, with the research community setting up a

lead university with a hub and spoke model, similar to the NSTC, to assure that the fundamental research needs of the COE are met, as well as working with commercial innovation activities in companies including start-ups. The key would be to provide a smooth end-to-end glide path for relevant research into production, moving through all the stages from high-risk innovation to well-established processes, material, equipment and ecosystems.

Each COE would have a specific technology focus as described above and would manage a set of programs and projects to achieve the goal of accelerating the development of new packaging technologies and transferring this capability to the pilot lines for preparation for domestic manufacturing. Focused COEs are the fastest way to get technologies proven in. In addition, the COEs, using their associated pilot lines, would have an open interface to university and commercial research to transition a lab demonstration to a full technology capability demonstration. The appropriate pilot line would have a "research annex" which would accept experimental work in an earlier stage with less restrictions on wafer size etc. The COE would be tasked to encourage research work in its field of technology and support promising ideas to where they could be seriously considered for technology transfer to manufacturing.

Each NAPMP COE and pilot line would seek funding from the locations where they are located, including state funds, company partnerships, and other government grants to support their programs and activities, while intellectual property and licensing agreements would need to be uniform across all COEs in the NAPMP and NSTC. These agreements will have to be developed by the Public Private Partnership managing the NSTC/NAPMP along with NIST and the DOC.

Intellectual Property Ownership

(IP should be as common as possible with the NSTC but this section reflects the NAPMP position)

Generally, intellectual property (IP) should be owned by the researchers and companies generating the IP, not by the NAPMP. A robust IP framework is critical to the NAPMP's long-term successful operation and long-term self-sustainability.

The IP framework for ownership and licensing should lower the barrier to entry for start-ups and to enable university access. The NAPMP should, however, more broadly license participating and contributing members than directly funded US programs, because the NAPMP should be given a mission to share know-how, encourage collaboration, and sustain the R&D with private contributions. This framework will help the NAPMP fulfill its goals: allow partners to collaborate on R&D challenges and drive towards prototypes; promote the growth and nurture of startups; and accommodate the different needs of universities.

The IP framework adopted by the NAPMP should differentiate based on the type of project: whether it qualifies as pre-competitive/early-stage research or late-stage prototyping. The NAPMP should develop and publish criteria for the project type, adjust funding levels based on the type, as well as consider the scope of expected benefits and alignment with NAPMP's goals. Such a framework should encourage broad participation, recognize contributions, promote the publication of early-stage research, orchestrate access to the COEs for such research and prototyping collaborations that reduce barriers of entry, while providing licenses to participating and contributing members on reasonable terms.

Technology Transfer to Manufacturing; Pilot Lines

This is probably the most difficult challenge facing the NAPMP given the paucity of packaging production in the US, the capability of the Asian OSATs and the satisfaction of their customers with their performance. However, without a clear and high-confidence plan to transfer development to manufacturing in the US, the NAPMP will not be effective in creating manufacturing jobs. As a first step the NAPMP needs to engage likely potential companies in the following spaces to determine what they would need from the NAPMP that would help them to decide to manufacture in the US, which would largely determine how best to transfer technology to commercial realization.

High volume internal use: *Intel, Micron, Automotive, 6G Base station (Ericsson?)*
High volume package foundries: *Intel, GlobalFoundries, Samsung, TSMC*
Low volume internal/foundry: *Northrup, Boeing, Raytheon, General Electric, NHanced Semi, SkyWater, Integra Technologies*
Printed wiring board assembly: *Jabil, Sanmina etc.*

The NAPMP pilot lines would be responsible for merging the requirements of end products with the innovations from the COEs to develop reliable, high yielding and manufacturable processes. This requires that the pilot lines are aligned with facilities that can ramp production for end products. They would also have a key responsibility to support promising start-up companies with their early-stage manufacturing. The equipment required for advanced semiconductor packaging can be prohibitively expensive for small companies and the NAPMP pilot line can provide an initial path for early production.

The pilot lines would shake down the COE technology developments, prepare them for manufacturing and to support technology transfer to US based packaging manufacturing facilities including:

1. Support NSTC vertical COEs by producing the COE demonstrators.

2. De-risk advanced packaging manufacturing for companies seeking to expand or start packaging in the US including start-up enterprises and assembly companies integrating backwards to heterogeneous packaging.

3. Demonstrate how advanced packaging technologies can be economically manufactured in the US by revolutionary changes in the cost structure for substrate, assembly and test technologies and to allocate space for equipment companies to integrate their equipment into both existing and next generation process flows.

4. Provide companies with private space to develop and test proprietary packaging technologies.

5. Develop integration flows and test vehicles, control monitors, process control and productivity optimization analytics, measure reliability and develop quality metrics.

6. Provide technology transfer packages to industry including a full suite of materials, processes, equipment and test methods to create a smooth transition for products from development to commercial volume production.

7. Create an environment where advanced test technologies can be demonstrated on products that will ramp into production.

We recommend the following structure for pilot lines in the NAPMP:

1. Assembly and Test (A&T) Pilot Lines

In addition to the COE capabilities, three more expansive (in terms of manufacturing demonstrations) assembly and test pilot lines should be formed that would be capable of integrating various new packaging technologies such as hybrid bonding, heterogeneous integration, advanced SIPs, substrates, test and metrology into fully integrated electronic modules demonstrated at yield. The three pilot lines would be divided between the three different assembly technologies: wafer based, panel based, unit based. As shown above, the unit-based pilot line responsibility would be split into two separate pilot lines. The first would address the more flexible, heterogeneous needs of assembly and test for programs such as RF. The second would focus on more dense module packaging involving mixed signal analog modules. These two applications are sufficiently different and as such separate pilot lines are more optimal.

Each of these packaging technologies uses a different substrate format and hence different assembly tools and they have different facility requirements (cleanliness, vibration, chemicals, waste, etc.). Any final product could utilize all three (or any combination) of these assembly facilities. For example, wafer assembly can link two active die with interconnection densities approaching 1 million bonds per square mm with low pJ/bit energy consumption. In products having multiple die generating larger amounts of heat, a side by side configuration with low latency, high bandwidth interconnect schemes is required, enabled with advanced substrate technologies built at the panel level. Product level thermal solutions require processing at the unit level.

The location for the pilot lines is yet to be determined but would take advantage of existing facilities by being placed in conjunction with an existing commercial packaging facility in the US. Since there is little time to build a new green field location, we recommend that one A&T NAPMP pilot line be located with the proposed new Manufacturing Institute for Factory 4.0/5.0 for packaging. This would allow the Manufacturing Institute to work closely with the NAPMP COEs for equipment and use that pilot line as a testbed for its automation developments, including automated preventative maintenance to reduce human activity in the clean rooms. Since packaging is presently less automated than the frontend fabs, this offers significant opportunities for enhancement and cost reduction. Analytics for process and product anomaly detection, anomaly diagnosis, operations prediction and optimization in use in semiconductor fabs must be assessed for packaging use. Additional packaging specific analytics requirements should be identified and addressed.

2. Flex/Additive Pilot Line

This would be located at the existing NextFlex Manufacturing Institute facility in San Jose and would have the same objectives as the assembly and test line described above.

The pilot lines need to strike a balance between operating as a pre-production facility and flexibility to continuously incorporate new technologies and processes as developed by the COEs. These facilities need to emphasize batch processing and automation to enable economic commercial domestic production.

It is important to mention that these pilot lines would only engage in developing manufacturing capability. They would not engage in commercial activities that would compete with existing US packaging companies. The existing domestic packaging industry is small. The NAPMP must work to encourage and augment the existing industry. Failure to work with existing businesses would be counterproductive to the program goals.

How the NAPMP Organizations Collaborate with the NIST, NSTC, Manufacturing Institutes, Universities, and Other Government Funded Packaging R&D Organizations

The NAPMP should actively work to collaborate with other entities as follows:

1. Research organizations including universities, established and start-up companies and government labs

Each COE will be proactive in planning and supporting promising research ideas from universities and other organizations by (i) hosting road mapping and planning meetings, (ii) providing funding for joint programs and (iii) flexible access to facilities, equipment, metrology and technical advice to evaluate research results. It is also recommended that each COE would identify a lead university with broad skills and research in the area of the COE, and that this lead university would assist in creating a hub of other research universities to work with the COE. The COEs would assign a Chief Scientist or equivalent, whose task would be to interface with US based research and innovation organizations and assure that there was a close partnership with the NAPMP COEs and pilot lines.

Pre-competitive research should encourage collaborative projects involving a range of interested researchers from public and private entities, with goals spanning multiple years of effort. The NAPMP should emphasize these types of projects and orchestrate such efforts in its COEs. The COEs can leverage existing infrastructure, augmenting as necessary regional and university infrastructure, and include virtual participation capabilities so membership can be from all regions.

The NAPMP COEs should seek out the best institutions in allied countries to enhance the overall innovation effort and collaborate with and leverage these facilities if it is to the advantage of the NAPMP and the US.

2. Manufacturing Institutes

The Manufacturing USA Institutes are widely dispersed across the US, and it is expected that the NAPMP may collaborate with several of these organizations. As mentioned earlier in this white paper, the NAPMP would specifically utilize two existing Manufacturing Institutes as COEs – AIM Photonics and NextFlex since their established skills and facilities need not be duplicated and a new one recommended for factory automation.

Combining die from multiple digital and analog technology nodes, different functionality (memory, compute, sensors) creates a significant challenge to ensure functionality and achieve the low defect levels required for products. Test (functional, performance, system, etc.) is an area that needs focus, attention and development. Without quality, there is no product. Moreover, test technology needs to be closely aligned with product design and design tools to shift as much of the validation into the design phase as possible. Creating a Manufacturing USA institute focused on enabling "1+ Trillion Transistor" testing capability will create a domestic ecosystem to accelerate and drive innovation in this area.

3. Microelectronics (ME) Commons

The ME Commons program initiated by the Department of Defense is designed to bridge the Valley of Death for microelectronics of interest by forming a set of Regional Hubs (groups of universities with microelectronics research) with Cores (organizations with production capability). It will be closely linked with the NIST/DOC Chips ACT R&D support as shown on the following page:

DOC Programs	DOD Microelectronic Commons
Support growth of domestic capacity, capability for US commercial market	Ensure that growth supports, and takes advantage of, national defense technologies
CHIPS for America R&D	**Regional Hubs**
• NSTC - Supports the future market for, leading edge, heterogeneous integration, non-CMOS • NAPMP – Supports the future market for heterogeneous integration, advanced packaging • Mfg USA, NIST Metrology - Support the industry with manufacturing solutions and characterization methods	• Distributed network of technology-focused hubs that build on regional strengths • Support prototyping, leverage unique capabilities • Guided by national defense needs, projects proposed by hubs foster the best solutions
Incentives	**Cores**
Expanded capability and capacity to support high TRL / MRL development • High-TRL prototyping • Pilot, manufacturing processes • Test and assembly	• Commercial fabs and foundries • Mid-TRL prototyping, pilot, test and assembly through Commons • High TRL production and commercialization for DIB, services & others

Shared resources, network access, coordination, and planning

4. Commercial Companies

The NAPMP would be active in interacting with commercial companies including:

- Start-ups
- Established semiconductor and semiconductor ecosystem centric companies
- Companies presently engaged in electronics assembly which will be impacted by 3D HI and SiP packaging

It would use these interfaces to better understand the technical and product needs of the companies, to build technology roadmaps and to assure that the COE development programs are aligned with commercial needs. The NAPMP would support commercial companies in several ways: (i) de-risk new manufacturing, (ii) provide "private" facilities in the pilot lines for companies wishing to do proprietary development and (iii) provide access to equipment that companies need to complete their development and demonstrate performance in a full slow process.

The NAPMP should consider setting up a commercial outreach organization that is specifically assigned to support commercial companies – both small and large – to assure that any required consulting, technical support or pilot manufacturing is well managed.

5. Environmental Stewardship and Sustainability

The NAPMP will elevate the importance of environmental stewardship and sustainability in the advanced semiconductor packaging ecosystem by promoting the insertion and replacement of less sustainable integration flows with environmentally friendly, recyclable materials integration processes. This effort would include programs to develop more efficient, less wasteful techniques focused on minimization of materials consumption. Such a program can also include the conservation and reduced consumption of strategic materials, including rare earth elements and conflict minerals (metals). Additional areas of focus will include the elimination of chemical emissions into the atmosphere, water and soil through waste reduction, selective removal, purification and circular chemical

solutions. As such, NAPMP recognizes a strong need for a cross-cutting advanced materials development collaboration with US-based universities and materials suppliers.

6. Other Government Programs

In the area of advanced semiconductor packaging, the NAPMP would seek to collaborate with other government funded efforts such as NIST, National Labs, DARPA, etc. The overall NSTC/NAPMP technical Advisory Board would have oversight to assure that there was efficient collaboration and minimize wasteful duplication.

Success Metrics

It is important that the progress, effectiveness, and success of the NAPMP organization is tracked with quantitative metrics. However, it must also be considered that some of the higher-level metrics like US share of semiconductor package production have many factors that are beyond the control of the NAPMP, including commercial decisions made by companies. In addition, the success metrics need to include a mix of leading and trailing indicators to assure that a full picture of the NAPMP success is available. A proposed set of metrics is shown below in the table below, broken down into four categories – operations, technical, economic and workforce development.

Operations	• # of NAPMP projects taken to production in USA • # of members and dues paid • # of projects delivered on schedule • # of projects transfer to manufacturing	• Budget control • # of research partnerships (academic and commercial) • Progress towards industry self sufficiency for the NAPMP • Assess performance of each NAPMP COE
Technical	• Roadmap acceleration versus prior expectations • US technical leadership • # of technologies/processes/products transferred to manufacturing • Reduced environmental footprint for packaging technologies	• # of breakthrough challenges supported by NAPMP developed technologies • # of projects terminated for technical reasons • # of patents and license revenue • # of peer reviewed papers and conference presentations
Economic	• US production market share in semi packaging (advanced and mature) • # of new jobs created in US packaging facilities • Growth of new industries supported by the NAPMP (eg EV, medical etc) • Growth of US based packaging foundry	• # of start-up companies supported by NAPMP • # of packaging related start-ups reaching successful exit • National security support • # of projects terminated for market reasons • Improved supply chain resilience (less dependence on Taiwan)
Workforce	• # of students in training versus goals (AA, BS, MS, PhD) • % minority and retrained students (eg military) • # of students hired by semiconductor packaging industry • # of semi packaging centric locations, courses and programs • Geographic diversity of training	• % students graduating in 2 years (CC) and 4 years (BS) • # students hired by semi-industry • Number of CCs, colleges, and universities offering courses. • # of student internships (at multiple levels: 2-year, 4-year, post -grad)

Financial Sustainability

While a five year appropriation of funding may not be sufficiently long, neither is an unlimited supply of government support desirable or appropriate. By comparison with other successful semiconductor alliances in Europe (imec, Fraunhofer, LETI) it is apparent that a steady state of 25% government funding (federal, state and local) and 75% industry funding appears to be optimum. This should be the target prior to the end of year ten with the major portion of the budget for the NAPMP being borne by its commercial customers. One benefit of some continuing government support means that smaller and newer companies can be part of the organization before they reach financial stability. Industry and other sources of funding would come from industry supported programs and projects, license fees, services, etc.

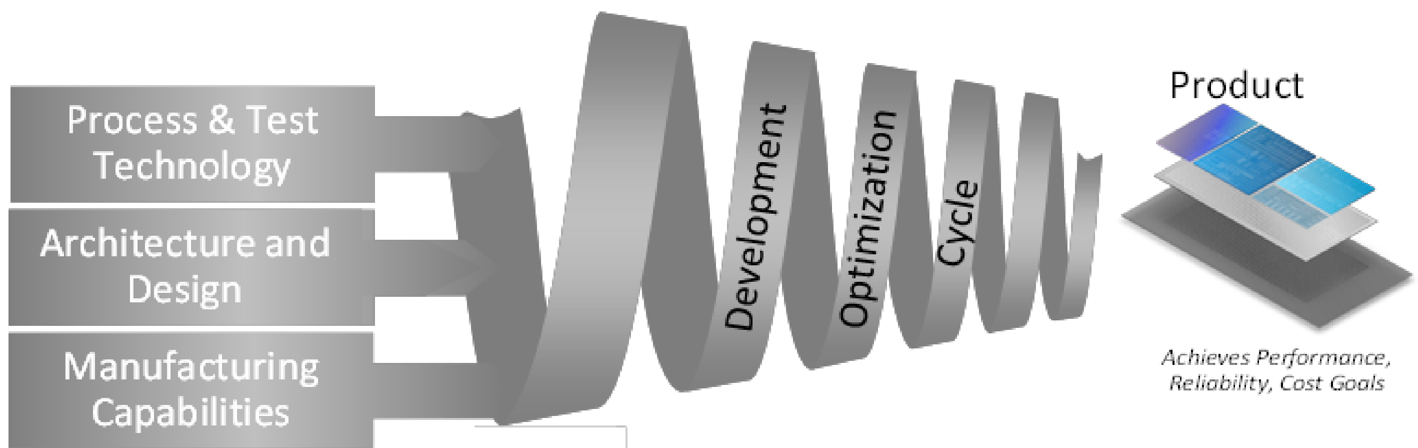
Workforce Development

The NAPMP would participate in the broader NSTC/NAPMP/industry effort on enhancing workforce development. The lack of detail in this white paper in no way reflects a lack of interest or support, but rather one of delegation since the workforce program needs to spread across multiple entities. The NAPMP COEs and pilot lines would be ideally positioned to support as the facilities of both the COEs and pilot lines would provide an excellent location for internships and apprenticeships to train workers for production and engineering jobs. The distributed nature of the COEs and pilot lines would allow multiple locations around the US to be involved. The facilities would also be involved in helping universities, including HBCUs, and community colleges near their locations to build classes related to semiconductor packaging along with hands on experience and labs.

Summary

The formation of the NAPMP is critical for the recovery of advanced semiconductor packaging technology and manufacturing in the US. This white paper proposes that several program and project focused COEs be formed around the new technologies in packaging along with five pilot lines to interact with research organizations, accelerate technology development and transfer these technologies into economic and sustainable manufacture in the United States. These advanced packaging technologies will enable multiple rapidly expanding markets thereby increasing the economic and national security of the nation.

However advanced packaging, where multiple chips can be interconnected into one package, requires evolutionary and revolutionary improvements in product design, process flow, manufacturing and product test. This requires a very tight optimization to meet product performance, reliability and cost targets as illustrated below and the NAPMP programs need to be closely linked, and also with the NSTC.



Again, we recommend the NAPMP collaborates with university and commercial research for NSTC entities and other government supported activities such as NIST. The NAPMP will work with the NSTC to build a national workforce development program using its facilities to offer intern and apprenticeship opportunities to build the skilled workforce that will be required for manufacturing in the US.